Nanotechnology Fueling Moore's Law

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Outline

- Key Messages
- What is Nanotechnology?
- Nanotech State of the Art
- The Future
- The Ultimate Vision
- Summary
- Q+A

Key Messages

- Nanotechnology is here today in "state of the art" high speed Si CMOS process technologies
- Si nanotechnology process scaling/convergence will continue for the next 10-15 years
- Alternative new technologies have emerged and will begin to be integrated into Si CMOS by 2015
- Nanoscience research is needed to facilitate these radical new scalable technologies beyond 2020

What is Nanotechnology?

a. New structures like carbon nanotubes
b. Silicon devices made smaller
c. Arranging atoms and molecules
d. Letting atoms assemble themselves
e. Something far in the future
f. In production today
g. All of the above

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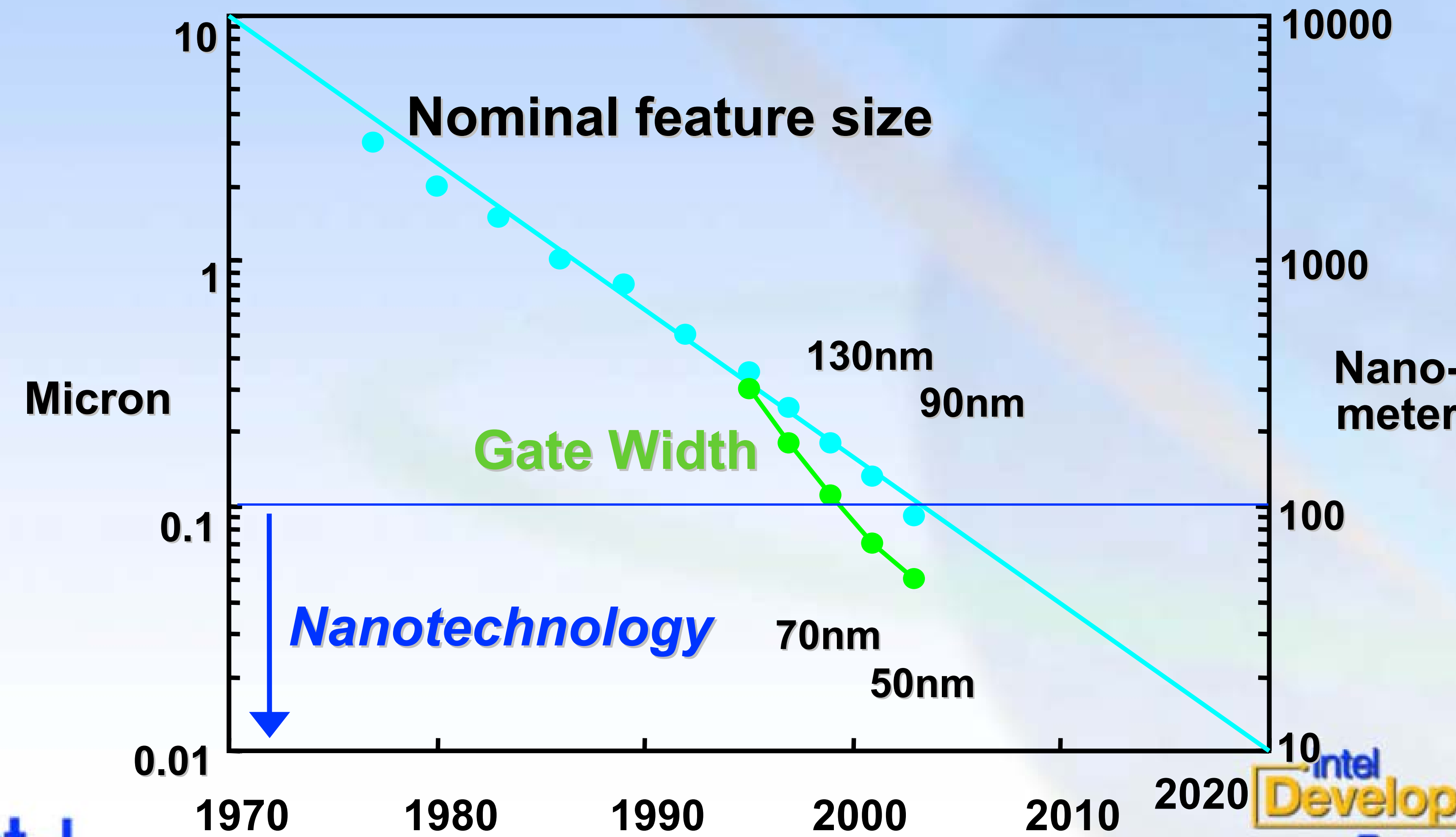
NSET* Nanotechnology Definition (Feb 2000)

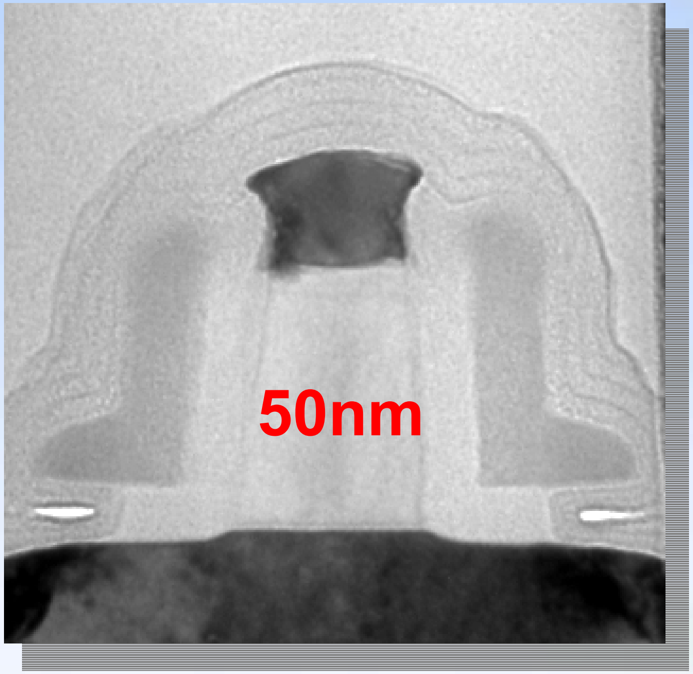
Research and technology development at the atomic, molecular, or macromolecular levels, in the length scale of approximately 1 – 100 nanometer range

*National Science and Engineering Technology Council

Silicon Nanotechnology is Here!

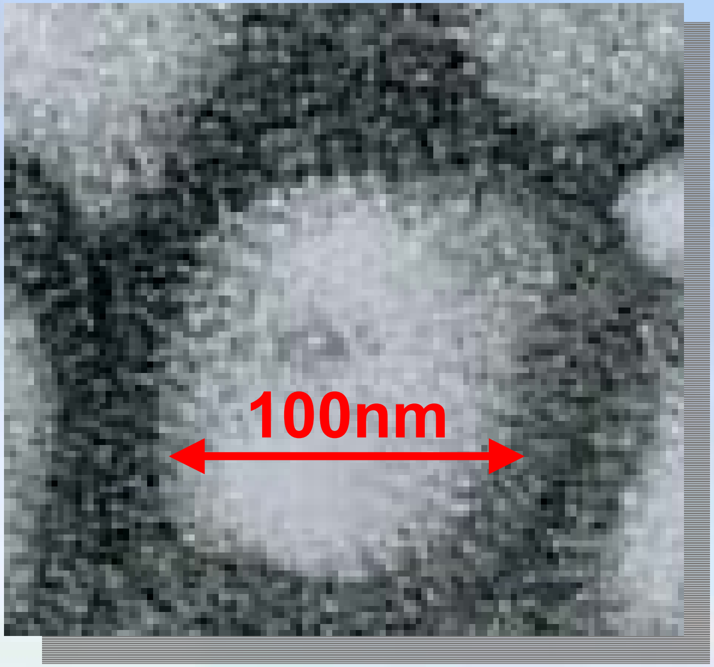


Silicon Devices Shrink to Virus Size



Transistor for 90nm Process

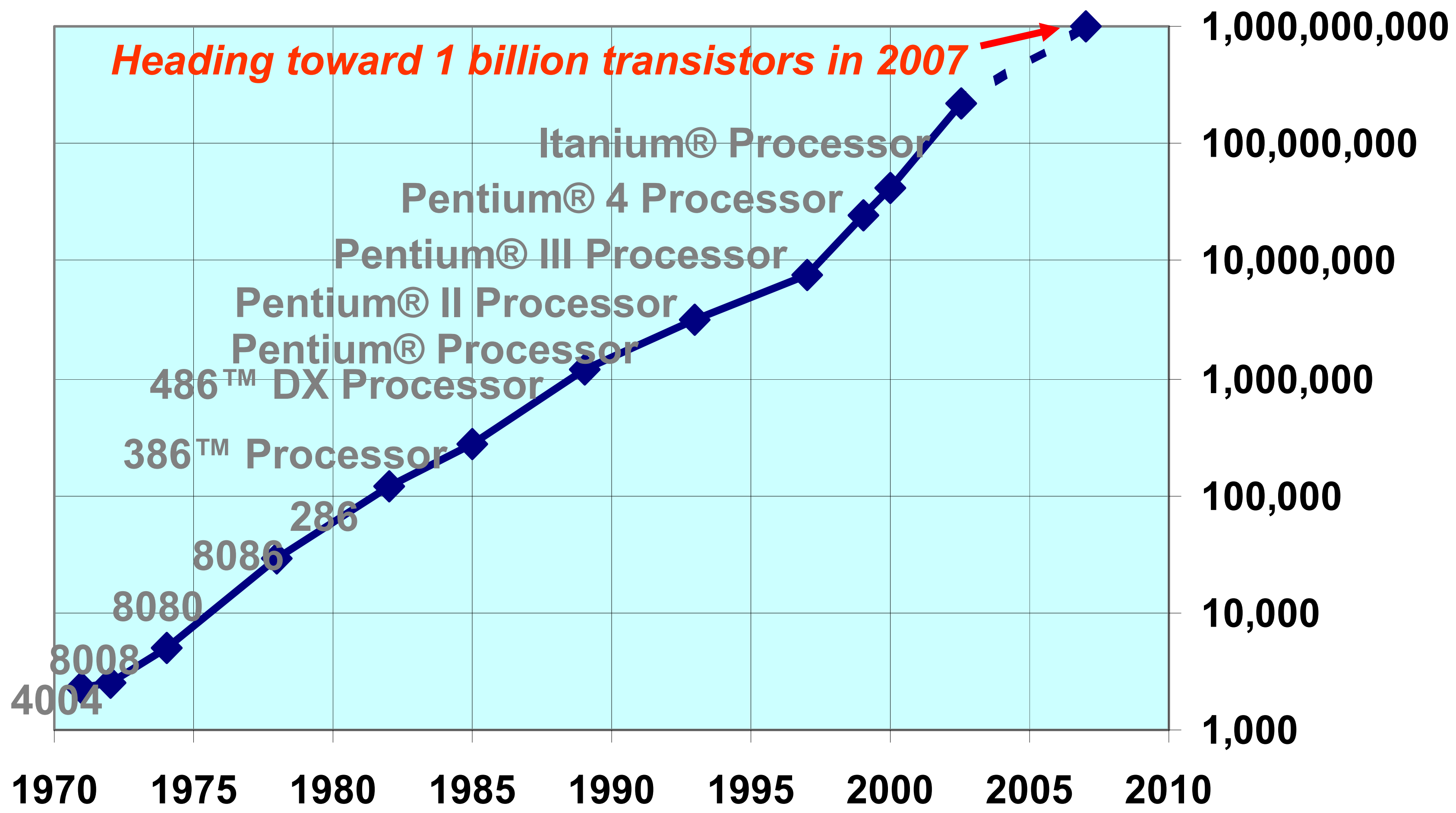
Source: Intel



Influenza virus

Source: CDC

Moore's Law In Action



>220M Transistors Integrated Into Devices Produced Today

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>6 Orders Of Magnitude Reduction in Cost/Transistor

Source: WSTS/Dataquest/Intel, 8/02

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New Materials, Devices Extend Si Scaling

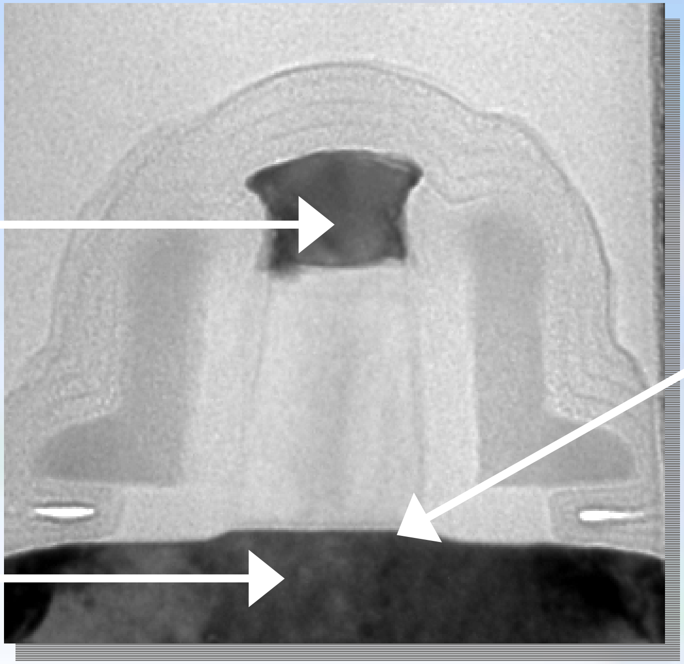
Changes Made

Gate

Silicide added

Channel

Strained silicon



Transistor

Future Options

High-k gate dielectric

New transistor structure

Source: Intel

New Materials, Devices Extend Si Scaling

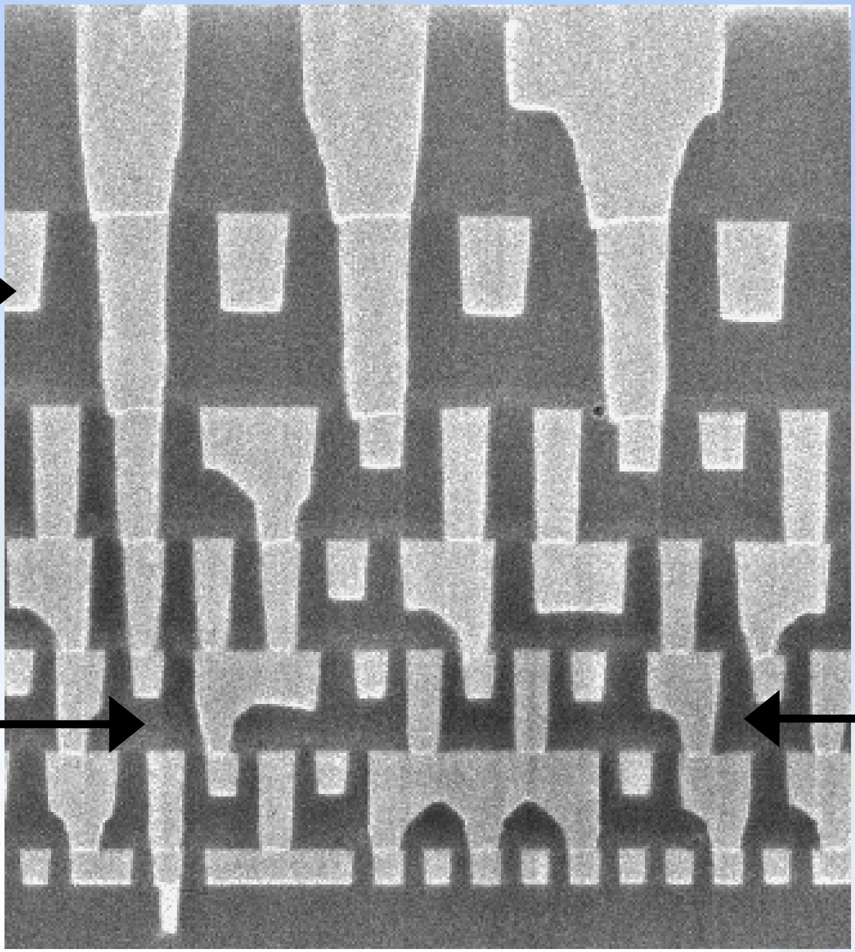
Changes Made

Metal lines

Al → Cu

Insulating dielectric

SiO_2 → SiOF → CDO (low-k)



Interconnects

Source: Intel

Future Options

Ultra Low-k Dielectric

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The Future

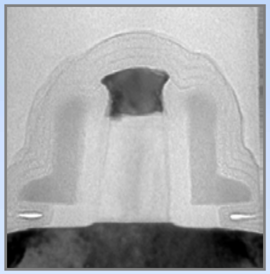
- Continue CMOS Nanoscaling
- Non-classical CMOS
- Convergence
- Novel devices

Nanotechnology features

- Structures measured in nanometers
  - Less than 0.1-micron (100nm)
- New materials and device structures
  - Incrementally changing silicon technology base
- Materials manipulated on atomic scale
  - In one or more dimensions
- Increasing use of self-assembly
  - Using chemical properties to form structures

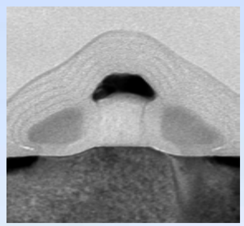
Intel Nano Transistors

**90nm Node
2003**



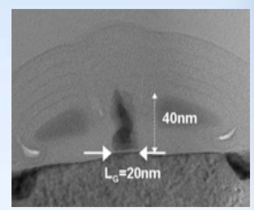
50nm Length
(IEDM2002)

**65nm Node
2005**



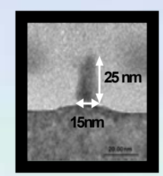
30nm Prototype
(IEDM2000)

**45nm Node
2007**



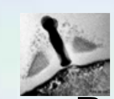
20nm Prototype
(VLSI2001)

**32nm Node
2009**



15nm Prototype
(IEDM2001)

**22nm Node
2011**



10nm Prototype
(ITJ 2002)

Increasing leakage

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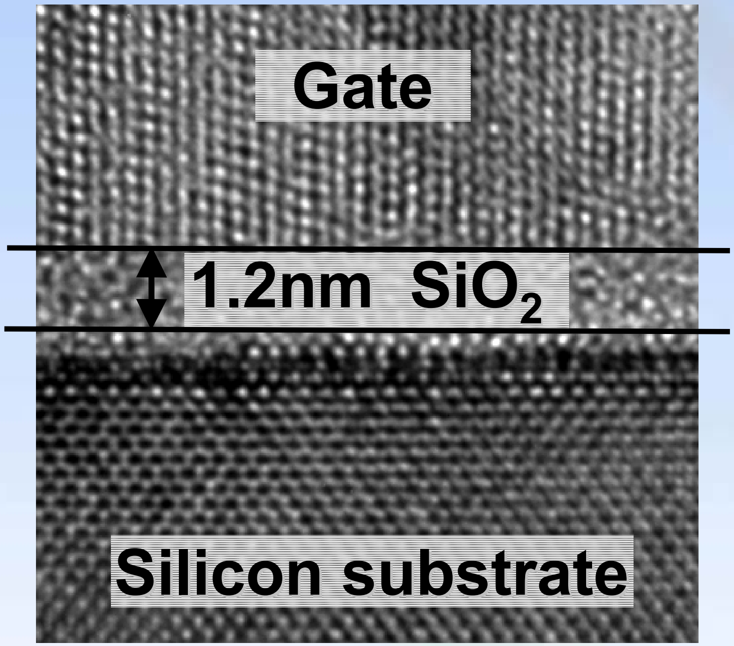
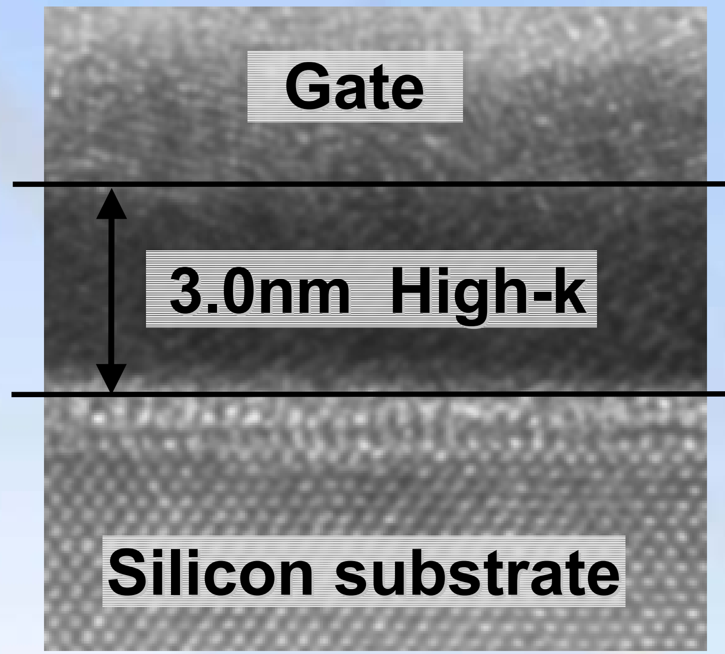
Nanotechnology for Gate Dielectrics



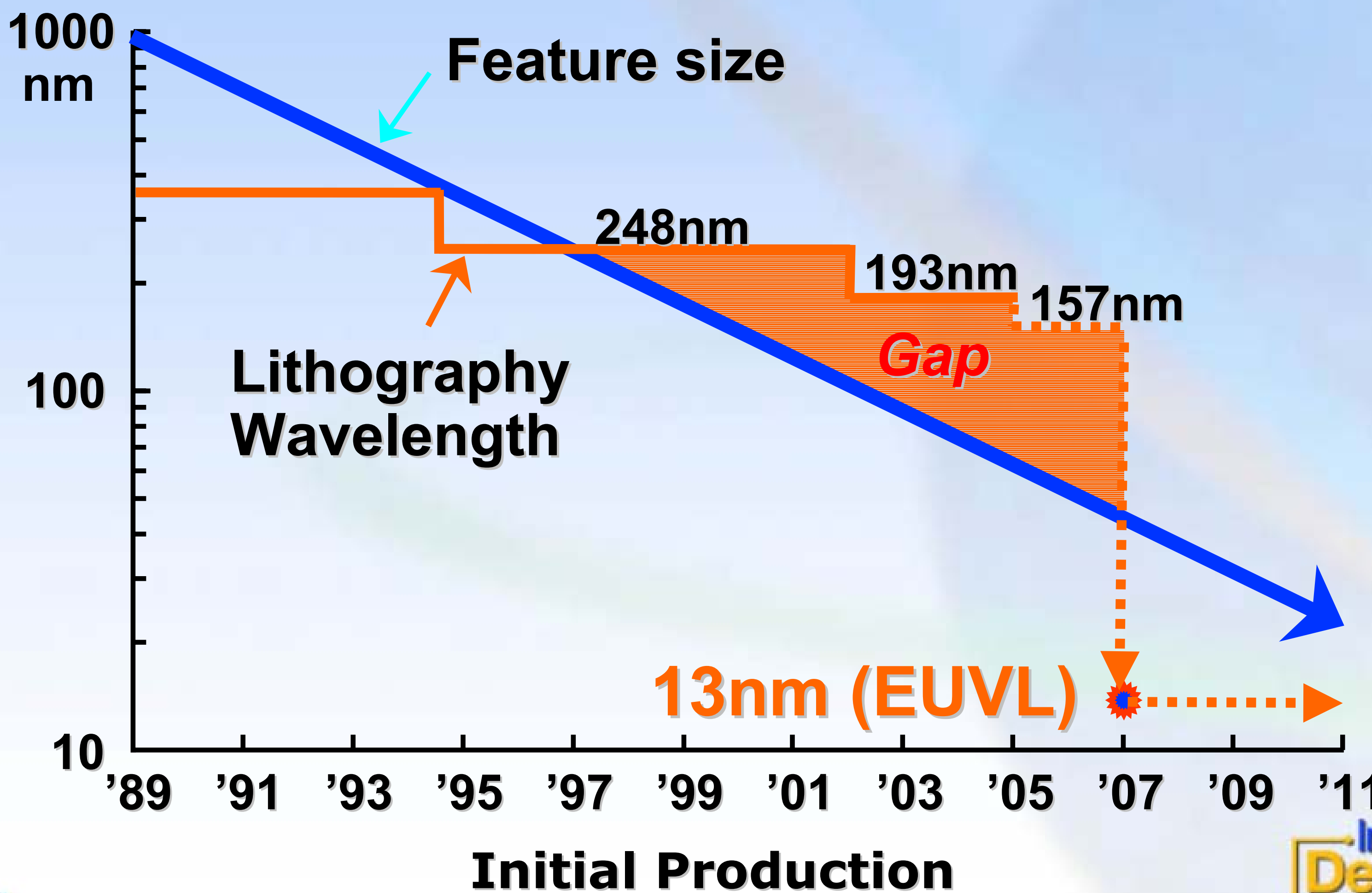


Source: Intel

	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Integration is the key challenge

Lithography Gap to Close with EUVL



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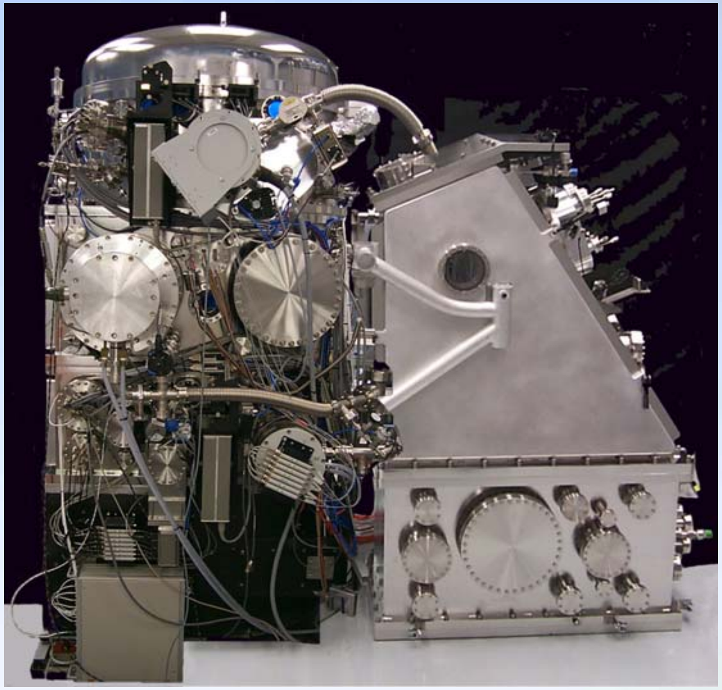
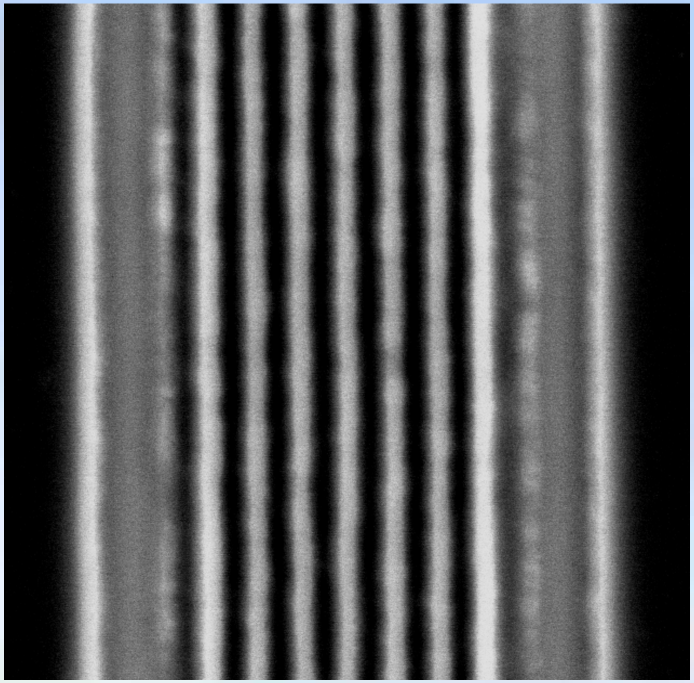
EUV LLC Consortium Demonstrates EUVL



EUV Lithography Prototype Exposure Tool



50nm Lines Printed with EUV Lithography

EUV lithography is now in commercialization phase

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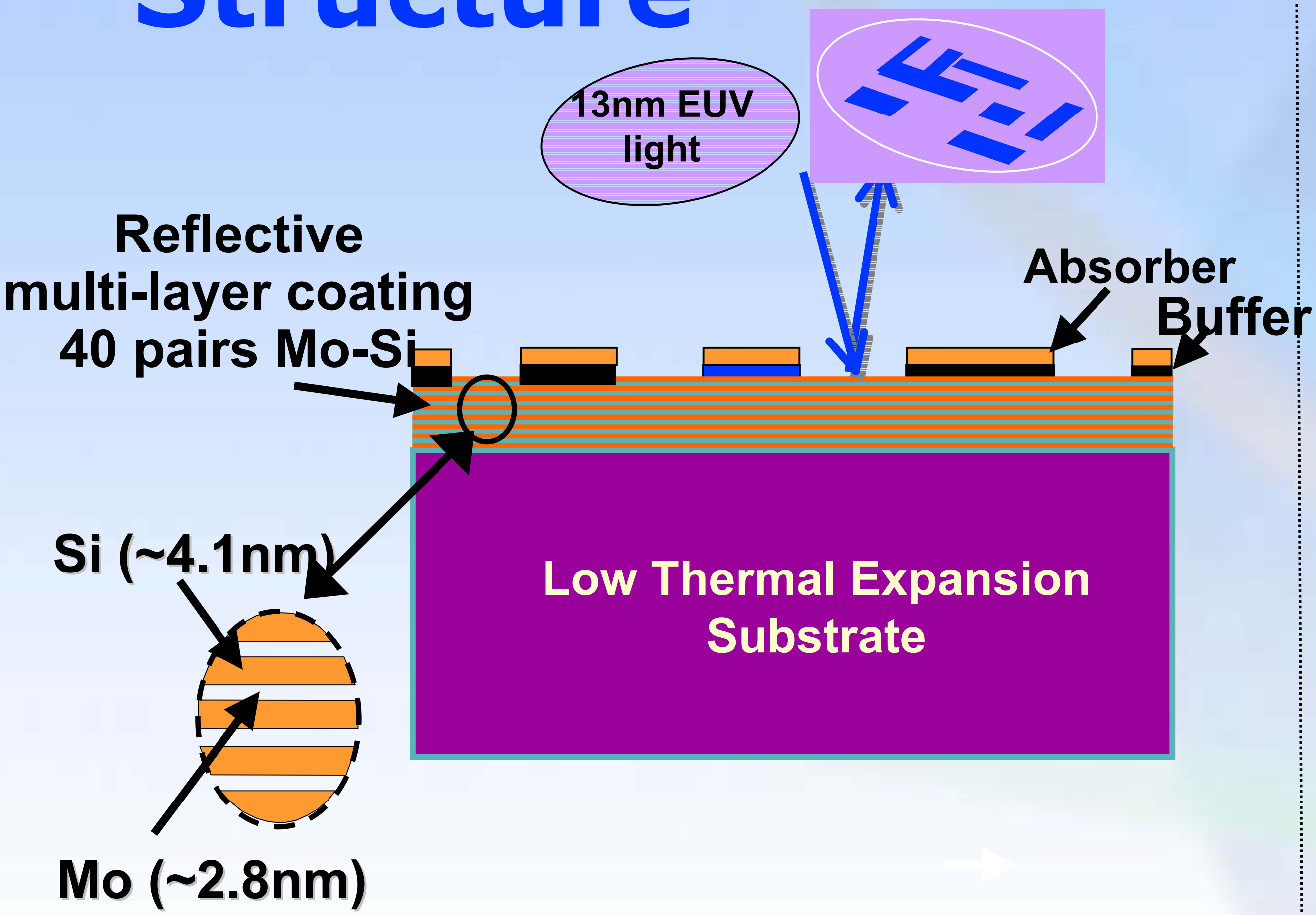
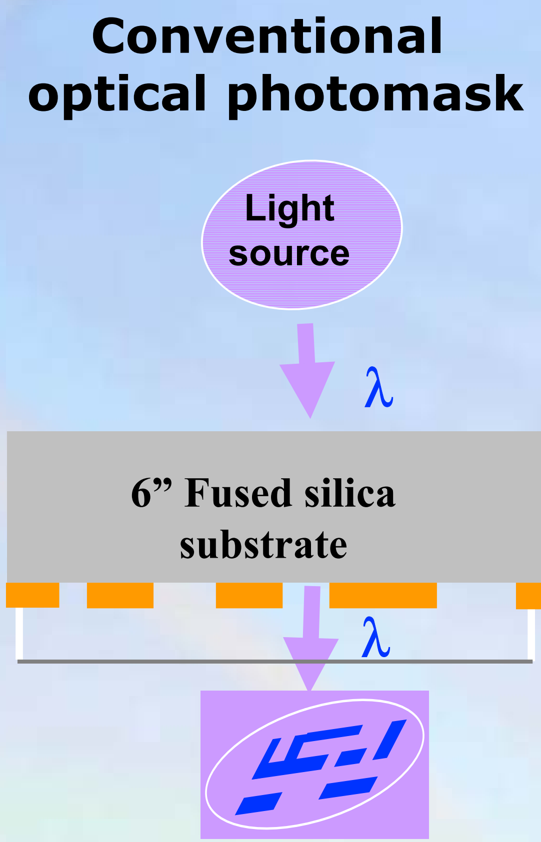
Source: Sandia

EUV Reflective Mask Structure



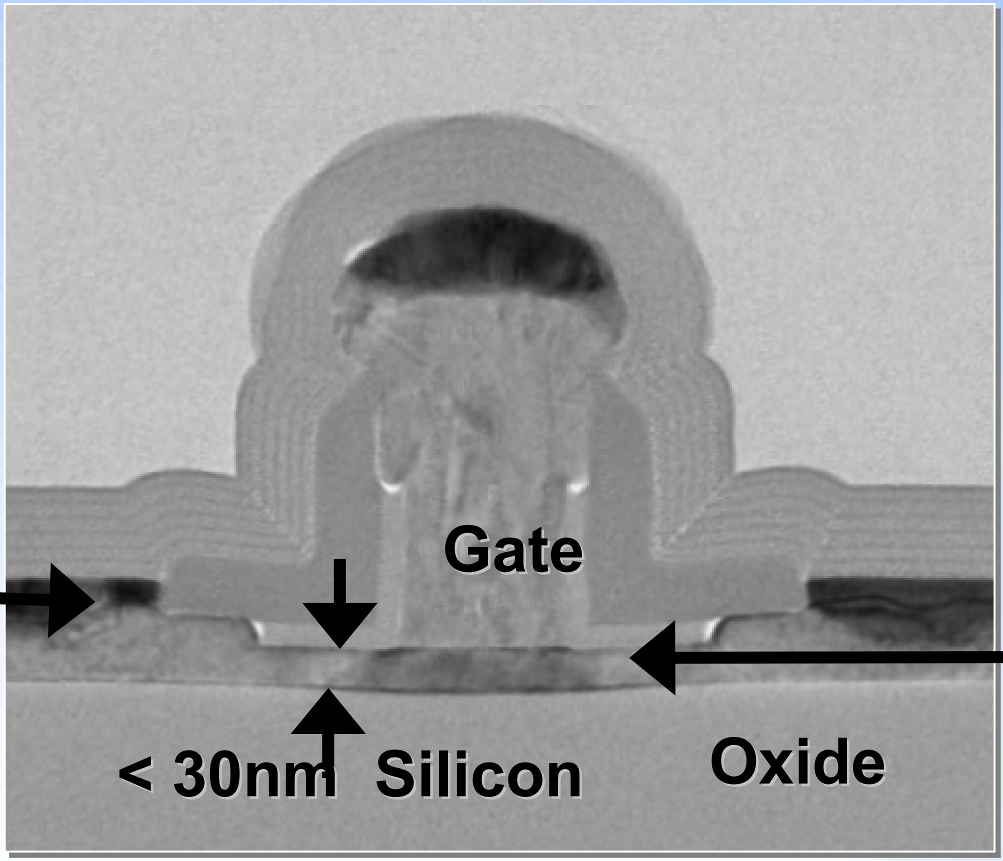


The Future

- Continue CMOS Nanoscaling
- Non-classical CMOS
- Convergence
- Novel devices

Intel's TeraHertz Transistor: Lower I_{off} Leakage

Raised Source/ Drain



High-k Gate Dielectric

Fully Depleted Substrate: Subthreshold Leakage is Approaching Theoretical Minimum

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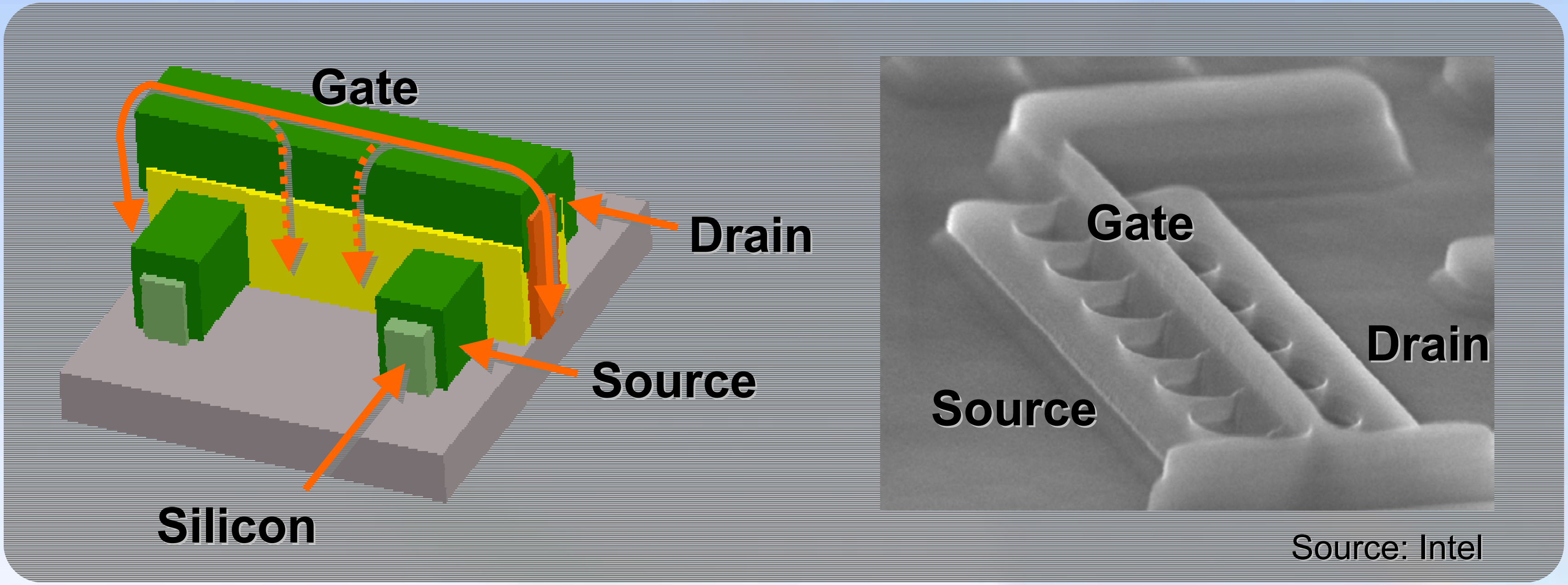
Experimental Tri-Gate Transistor

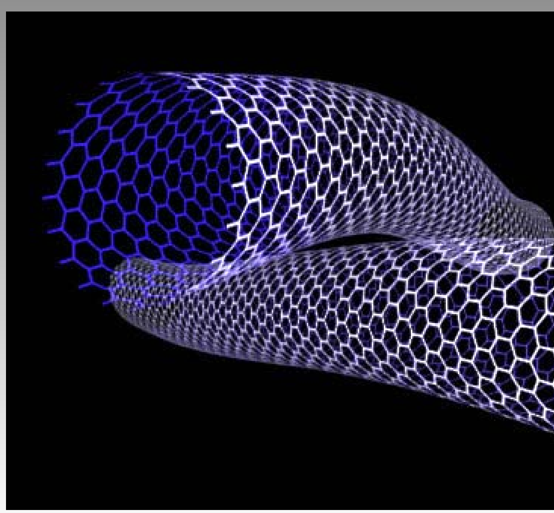


- **Improved version of TeraHertz transistor**
  - **Better performance**
  - **Scalable to smaller sizes (low leakage)**
  - **Possible intercept towards end of decade?**

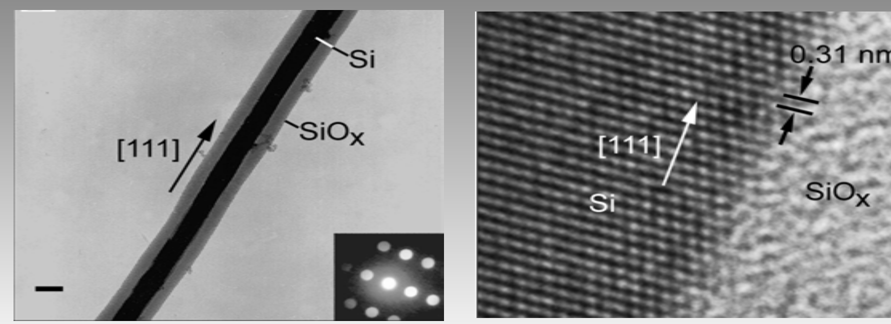
Nanotubes/Nanowires (>> 2010?)

- **Collaborations with universities in progress**
- **Good individual device data, many integration and materials issues to be resolved**

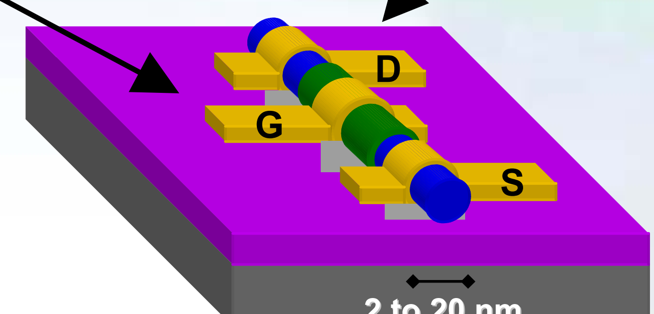
Carbon Nanotube



Silicon Nanowire



Source: Morales & Lieber, Science **279**, 208 (1998)



The Limits of Logic Scaling

- **For an *arbitrary* switching device made of of a single electron in a dual quantum well**
  - **Operating at room temperature**
- **It can be shown a power dissipation limit of 200 W/cm**2**
- **Will limit the operational frequency to ~100 GHz at length scales ~ 4 nm**

The Future

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Marriage of High Speed Logic with Other Technologies

- Flash/DRAM
- RF

{ Today

- MEMS/NEMS
- Optoelectronics
- Bioelectronics
- Alternate memory
  - MRAM, FeRAM, Ovonics

{ Future

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Intelligent Silicon

Nano is **Here**

New **Devices**,
Materials, and **Processes**

Expanding the Silicon **Canvas**

Silicon Innovation Enabling Convergence

The Future

- Continue CMOS nanoscaling
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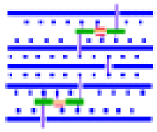
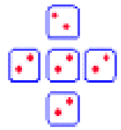
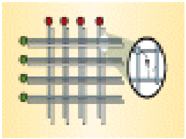
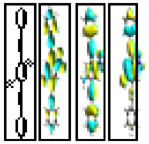
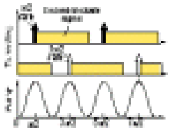
Novel Devices: R+D Time Requirements

- **Product development spectrum**
  - Software
  - System
  - Assembly
  - mArch
  - Power delivery and cooling
  - Circuit Design
  - Layout
  - Processing
  - Materials
- **Change that affects one level or two adjacent levels is relatively easy to manage → 2-5 years R+D effort**
- **Change that affects many levels is very difficult → 6 – 20 years R+D effort**
  - Must coordinate all changes
  - Long lead times

Emerging Research Architectures

						
ARCHITECTUR	3-D INTEGRATION	QUANTUM CELLULAR AUTOMATA	DEFECT TOLERANT ARCHITECTURE	MOLECULAR ARCHITECTU RE	CELLULAR NONLINEAR NETWORKS	QUANTUM COMPUTING
DEVICE IMPLEMENTATIO N	CMOS with dissimilar material systems	Arrays of quantum dots	Intelligently assembles nanodevices	Molecular switches and memories	Single electron array architectures	Spin resonance transistors, NMR devices, Single flux quantum devices
ADVANTAGES	Less interconnect delay, Enables mixed technology solutions	High functional density. No interconnects in signal path	Supports hardware with defect densities >50%	Supports memory based computing	Enables utilization of single electron devices at room temperature	Exponential performance scaling, Enables unbreakable cryptography
CHALLENGES	Heat removal, No design tools, Difficult test and measurement	Limited fan out, Dimensional control (low temperature operation), Sensitive to background charge	Requires pre-computing test	Limited functionality	Subject to background noise, Tight tolerances	Extreme application limitation, Extreme technology
ATURITY	Demonstration	Demonstration	Demonstration	Concept	Demonstration	Concept

~2009? ← 2015++ →

Technical criteria

- *CMOS compatibility*
- *Energy efficiency*
- *Scalability*
- *Performance*
- *Architectural compatibility*
- *Sensitivity to parametric variation*
- *Room temperature operation*
- *Stability and reliability*

Option Must Be Superior to Si CMOS Based On Cost, Power, Performance

The Ultimate Vision

The brain is the ultimate model for its ability to deal with complexity

- Little understanding on its architecture & organization
- Compared to tomorrow's computers
  - Orders of magnitude more powerful
  - Self assembled
  - Parallel operation
  - Self repairing to a significant degree
  - Fault tolerant
  - Runs on ~ 10W
  - 3D

Summary

- Nanotechnology is here today in "state of the art" high speed Si CMOS process technologies
- Si nanotechnology process scaling/convergence will continue for the next 10-15 years
- Alternative new technologies have emerged and will begin to be integrated into Si CMOS by 2015
- Nanoscience research is needed to facilitate these radical new scalable technologies beyond 2020